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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,403	01/09/2004	Takumi Yamaguchi	10873.1377US01	7971

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EXAMINER	
PETERSON, CHRISTOPHER K	
ART UNIT	PAPER NUMBER
2609	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/754,403	YAMAGUCHI ET AL.	
	Examiner	Art Unit	
	Christopher K. Peterson	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09 January 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 08 March 04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on March 8, 2004. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 4, 9 – 13, and 16 - 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibazaki (US Patent # 6,999,119) in view of Kijima (US Patent # 6,882,366).

As to claim 1, Shibazaki (Fig. 1) teaches a solid-state imaging device, comprising:

- an imaging region (image capturing element 10) in which a plurality of pixels (1) are arranged (Col. 11, line 56 – Col. 12, line 14);
- a signal line (vertical transfer circuits 2) through which a pixel signal of the imaging region (10) is read out (Col. 12, line 21 – 34),
- wherein an adding circuit (vertical transfer circuits 2) for adding pixel signals obtained from two or more of the pixels (1) is provided so that an output signal of the adding circuit is read out to the signal line (output signal 5) (Col. 13, line 38 – 51),

Shibazaki does not teach:

- wherein on the basis of a predetermined reference quantity of light incident onto the imaging region, a gain of the adding circuit in a condition in which a quantity of the incident light is above the reference quantity is controlled to be smaller than a gain of the adding circuit in a condition in which a quantity of the incident light is below the reference quantity.

Kijima (Fig. 1) teaches:

- wherein on the basis of a predetermined reference quantity of light (auto exposure control circuit 11) incident onto the imaging region (1), a gain (gain control amplifier (AMP) 3) of the adding circuit in a condition in which a quantity of the incident light is above the reference quantity (11) is controlled to be smaller than a gain (3) of the adding circuit in a condition in which a quantity of the incident light is below the reference quantity (11). Kijima teaches the auto

exposure control circuit provides a signal to the CPU (8), which in turn controls the gain of the gain control amplifier (Col. 13, line 14 – 51 of Kijima).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided the auto exposure control circuit (11) and gain control circuit (3) as taught by Kijima to the image capturing device (10) with adding circuits (2) of Shibazaki, because dynamic image processing improves the frame rate without the use of any high drive frequency. This makes it possible to be ready for still picture photography in a shorted period of time (Col. 3, line 18 – 67 of Kijima).

As to claim 2, this claim differs from claim 1 only in that the claim 2 recites the limitation of "wherein, within at least a partial range of a quantity of incident light onto the imaging region, a gain of the adding circuit is controlled to decrease with an increase of the quantity of the incident light". Kijima teaches the auto exposure control circuit provides a signal to the CPU (8), which in turn controls the gain of the gain control amplifier (Col. 13, line 14 – 51 of Kijima). Thus claim 2 is analyzed as previously discussed with respect to claim 1 above.

As to claim 3, Shibazaki teaches the solid-state imaging device according to claim 1, wherein the adding circuit (vertical transfer circuits 2) is arranged between the imaging region (image capturing element 10) and the signal line (output signal 5) (Col. 13, line 38 – 51).

As to claim 4, Shibazaki (Fig. 2) teaches the solid-state imaging device according to claim 1, wherein a plurality of the adding circuits is arranged between the two or more pixels (1a – 1d) included in the respective sets of pixels (Col. 13, line 52 – 62).

As to claim 9, Shibazaki teaches the solid-state imaging device according to claim 1, wherein when signals of N pieces of pixels (1a – 1d) are added, a gain (12) of the adding circuit is controlled so that an output value from the adding circuit is not more than a value obtained from the following formula: (value obtained by adding the N pieces of signals)/N (Col. 15, lines 25 – 38). The function of the formula above acts as an averaging function. Shibazaki teaches that the automatic gain control is implemented in correspondence to the sensitivity to the output signal. The photographing mode selector switch (25) determines the mode of the imaging device. The CPU 21 and the DSP 14 work together to control the average brightness level of the image dependent on the selected mode (Col. 20, line 14 – Col. 21, line 24).

As to claim 10, Shibazaki teaches solid-state imaging device according to claim 1, wherein when signals of N pieces of pixels (1a – 1d) are added, a gain (12) of the adding circuit is controlled so that an output value from the adding circuit is less than a value obtained by adding the N pieces of signals and more than a value obtained from the following formula: (value obtained by adding the N pieces of signals)/N (Col. 15, lines 25 – 38). The function of the formula above acts as an averaging function. Shibazaki teaches that the automatic gain control is implemented in correspondence to the sensitivity to the output signal. The photographing mode selector switch (25) determines the mode of the imaging device. The CPU 21 and the DSP 14 work together to control the average brightness level of the image dependent on the selected mode (Col. 20, line 14 – Col. 21, line 24).

As to claim 11 Shibazaki teaches a camera (31) equipped with the solid-state imaging device according to claim 1 (Col. 17, line 44 – 58).

As to claim 12, claim 12 is analyzed as previously discussed with respect to claim 3 above.

As to claim 13, claim 13 is analyzed as previously discussed with respect to claim 4 above.

As to claim 16, claim 16 is analyzed as previously discussed with respect to claim 9 above.

As to claim 17, claim 17 is analyzed as previously discussed with respect to claim 10 above.

As to claim 18, claim 18 is analyzed as previously discussed with respect to claim 11 above.

5. Claims 5, 8, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibazaki (US Patent # 6,999,119) and Kijima (US Patent # 6,882,366) as applied to claims 1 – 4, 9 – 13, and 16 - 18 above, and further in view of Trevino (US Patent Pub. # 2002/0012056).

As to claim 5, note the discussion of Shibazaki and Kijima above, Shibazaki and Kijima do not teach the gains for at least two of the plurality of adding circuits are controlled individually. Trevino teaches the gains for at least two of the plurality of adding circuits (focal plane processor 120) are controlled individually (Para 0036 - 0037). Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to have provided the gains for at least two of the plurality of adding circuits are controlled individually as taught by Trevino to the image capturing device of Shibazaki as modified by Kijima, to provide an improved sensor that would reduce memory storage and bandwidth requirements (Para 0010).

As to claim 8, Trevino teaches the adding circuit (focal plane processor 120) is provided with an averaging portion for averaging pixel signals obtained from two or more of the pixels (106), and when the quantity of incident light is larger than a predetermined higher reference quantity that is larger than the reference quantity, an output of the averaging portion is read out to the signal line in place of the added signal (Para 0037). Trevino teaches that the focal plane processor may be a time or special averaging circuit and that a pixel value can be changed depending on the pixel values of the surrounding pixels.

As to claim 14, claim 14 is analyzed as previously discussed with respect to claim 5 above.

As to claim 15, claim 15 is analyzed as previously discussed with respect to claim 8 above.

6. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibazaki (US Patent # 6,999,119) in view of Kijima (US Patent # 6,882,366), and further in view of Takayama (US Patent # 7,088,395).

As to claim 6, note the discussion of Shibazaki and Kijima above, Shibazaki and Kijima do not teach a photometer portion is provided between the imaging region and the signal line so as to detect a quantity of the incident light onto the imaging region. Takayama teaches a photometer portion (150b) is provided between the imaging region (54) and the signal line (w1 and w2) so as to detect a quantity of the incident light onto the imaging region (54). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a photometer portion is provided between the imaging region and the signal line so as to detect a quantity of the incident light onto the imaging region as taught by Takayama to the image capturing device of Shibazaki as modified by Kijima, because the image-capturing apparatus will reduce its power consumption, low-cost and reduce the number of necessary parts (Col. 2, line 62 – Col. 3, line 10 of Takayama).

As to claim 7, claim 7 cites a photometer portion is arranged between the two or more pixels as to claim 6. Takayama teaches a photometer portion (50b in Fig. 4) is arranged between the two or more pixels (50a).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nayar (US Patent # 7,084,905) is cited to teach method and apparatus for obtaining high dynamic range images.

Fossum (US Patent # 6,734,905) is cited to teach dynamic range extension for CMOS image sensors.

Johnson (US Patent # 6,252,536) is cited to teach dynamic range extender apparatus, system, and method for digital image receiver system.

Itani (US Patent # 6,707,492) is cited to teach successive approximation calibration apparatus, system, and method for dynamic range extender.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher K. Peterson whose telephone number is 571-270-1704. The examiner can normally be reached on Monday - Friday 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh D. Nguyen can be reached on 571-272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CKP
26 March 2007

CHANH D. NGUYEN
SUPERVISORY PATENT EXAMINER